Once the fine[,] or narrow band PLL has been tuned such that it [[is]] has been locked, its frequency may be used in conjunction with the frequency generated by the coarse PLL to provide channel tuning as previously described for the coarse/fine PLL tuning of FIGS. 21 and 22.

***In the Claims*:**

Please cancel claims 1-21, and add new claims 22-31.

1. (canceled)

2. (canceled)

3. (canceled)

4. (canceled)

5. (canceled)

6. (canceled)

7. (canceled)

8. (canceled)

9. (canceled)

10.(canceled)

11.(canceled)

12.(canceled)

13. (canceled)

14. (canceled)

15. (canceled)

16. (canceled)

17. (canceled)

18. canceled)

19. (canceled)

20. (canceled)

21. (canceled)

22. (new) An integrated VCO circuit comprising:

a VCO having a pair of driver transistors and a tank circuit; and

an adaptive bias circuit coupled to said driver transistors that maintains a nearly constant transconductance in said pair of driver transistors in response to changing temperature.

23. (new) The integrated VCO circuit of claim 22, wherein said adaptive bias circuit comprises:

a transconductance bias cell having an output that varies with temperature; and

an adaptive cell responsive to said output of said transconductance bias cell that provides a bias voltage to a gate of each of said pair of driver transistors.

24. (new) The integrated VCO circuit of claim 23, wherein the adaptive cell has a biasing transistor having a gate coupled to said output of said transconductance bias cell, a source coupled to a reference power supply, and a drain coupled to said gates of said driver transistors; and

wherein said biasing transistor is scaled to maintain a transconductance relationship characterized by $g_{mM1/M2} = k(g_{mM3})$;

wherein $g_{mM1/M2}$ is the transconductance of said pair of driver transistors, g_{mM3} is the transconductance of said biasing transistor, and k is defined by the operating characteristics of said transconductance bias cell.

25. (new) The integrated VCO circuit of claim 22, wherein said VCO and said adaptive bias circuit are disposed on a common substrate.

26. (new) The integrated VCO circuit of claim 22, wherein said adaptive bias circuit causes a gate-to-source voltage (V_{gs}) of said driver transistors to move in response to temperature variations.

27. (new) The integrated VCO circuit of claim 26, wherein said V_{gs} of said driver transistors are adjusted so to compensate for any transconductance variations that are caused by temperature variations of said VCO.

28. (new) An integrated VCO circuit comprising:

a VCO having a pair of driver transistors and a tank circuit; and

means for maintaining a constant transconductance of said pair of driver transistors.

29. (new) The integrated VCO circuit of claim 28, wherein said means for maintaining includes means for adjusting a gate-to-source voltage (V_{gs}) of said pair of driver transistors.

30. (new) The integrated VCO circuit of claim 28, wherein said means for maintaining includes: means for determining a temperature variation of said VCO; and

means for adjusting a bias voltage of said pair of driver transistors based on said temperature variation, so as to maintain a constant transconductance of said pair of driver transistors.

31. (new) The integrated VCO circuit of claim 28, wherein said means for maintaining includes:

means for adjusting a gate-to-source voltage of said pair of driver transistors based on said temperature variation, so as to maintain a constant transconductance of said pair of driver

transistors.